

## Analytical Method for Differential Amplifier Offset Voltage Analysis

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### Introduction

The operating precision of the most integrated circuits (IC) based on the differential amplifiers strongly depends on the input offset voltage of the differential amplifier. The continuous making efforts to develop the more precise analog IC's [1] call for investigations in field of differential amplifier offset voltage. The main purpose of the investigation, which is of great importance to the IC designers [2–4], is the determination of ways for offset voltage reduction.

The differential amplifier based on the bipolar junction transistors, which operate at high-current density, is analysed in the work. The results of theoretical investigation of offset voltage and recommendations for its reduction are presented. An analytical method based on the equations in the explicit form is used for this purpose.

### The basic equations

The junctions of the present-day bipolar junction transistors including those used in the differential amplifiers usually operate at high-current density, which corresponds to high-level injection of minority carriers [5]. The current density of the p-n junction depletion region operating at high-level injection can be presented by the following approximate equation [6, 7]

$$J = J_s \left[ \exp\left(-\frac{U_d}{V_T}\right) - \exp\left(-\frac{V_B}{V_T}\right) \right]^{-1}, \quad (1)$$

where  $J_s$  is the saturation current density of the junction,  $U_d$  is the voltage drop across the depletion region,  $V_T$  is the thermal voltage and  $V_B$  is the potential barrier of the junction. Equation (1) takes into account the main event caused by the high-level injection – the dependence of the majority carrier boundary concentrations on  $U_d$ . It should

be stressed that this equation does not take into consideration such effects as electron-hole scattering or dependence of  $V_B$  on  $U_d$ . The reason is that inclusion of these effects eliminates the possibility of obtaining the equation in explicit form.

At high-current density (at high-level injection) according to (1) the  $U_d$  is close to  $V_B$  and tends to  $V_B$  when the junction current increases. This phenomenon is indicated in a good many of books dedicated to semiconductor devices, e.g. [8]. It is explained by the fact that in case when  $U_d$  is close to  $V_B$  the barrier to the carrier flow is substantially reduced and large current may flow. Therefore,  $U_d \approx V_B$  in such a case and the depletion region in the equivalent circuit of the p-n junction can be presented as the voltage source  $V_B$ . Because of this, the voltage-current characteristic of the actual p-n junction at high-current density taking into the account the series resistance of the junction, which plays an important role in this junction operation mode, can be presented by a very approximate but simple equation

$$I_J = (U_A - V_B)/r_s, \quad (2)$$

where  $I_J$  and  $U_A$  are the junction current and voltage applied to the junction, respectively, and  $r_s$  is series resistance of the junction.

By applying of equation (2) for emitter junction, the collector current of the transistor operating in the forward active mode can be presented as follows

$$I_K = \beta (U_{BE} - V_{Be})/r_b, \quad (3)$$

where  $\beta$  is the forward current gain and  $r_b$  is the base series resistance of the transistor,  $U_{BE}$  is the voltage applied across the base-emitter and  $V_{Be}$  is the potential barrier of the emitter junction. Equation (3) is the base for the derivation of the equation of the input offset voltage.

It is necessary to stress that equation (3) is valid at high-current density and only in the narrow region of current, at which the differential amplifier input offset voltage measurement is provided and values of  $\beta$ ,  $r_b$  and  $V_{Be}$  can be considered as constants.

It should be mentioned that the widely used exponential (Shockley) equation of the junction does not allow us to obtain the equation of the input offset voltage in explicit form taking into the account the  $r_b$ .

### The input offset voltage analysis using analytical method

The circuit diagram of the differential amplifier is given in Fig. 1. It consists of the current source  $I_s$  and two arms, which contain elements  $V1$ ,  $R_1$  and  $V2$ ,  $R_2$ . The input offset voltage  $U_0$  is the voltage that must be fed between inputs ( $U_0 = U_{IN1} - U_{IN2}$ ) to make the output voltage  $U_{OUT1}$  equal to output voltage  $U_{OUT2}$ .

The arms of the differential amplifier of analogue IC are designed symmetrically and in the ideal case  $U_0=0$ . However,  $U_0$  is sensitive to dispersions of the element parameters that are unavoidable in the actual technology of IC [9–11]. Therefore, the arms become asymmetrical and actually  $U_0 \neq 0$ . The high value of  $U_0$  is often the main cause of low yield in the production of analog IC (e.g. in parallel analog-to-digital converters).

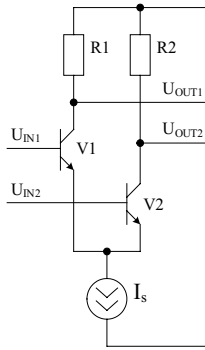


Fig. 1. The differential amplifier

The equation of the input offset voltage of the differential amplifier for the case when emitter junctions operate at high-current density derived using equation (3) is as follows

$$U_0 = \frac{r_b}{\beta R} \left( V_{Be1} R_1 \frac{\beta_1}{r_{b1}} - V_{Be2} R_2 \frac{\beta_2}{r_{b2}} \right) + \frac{r_b}{\beta R} \left( \frac{\beta_2 R_2}{r_{b2}} - \frac{\beta_1 R_1}{r_{b1}} \right) \frac{I_s r_{b1} r_{b2} + V_{Be1} \beta_1 r_{b2} + V_{Be2} \beta_2 r_{b1}}{\beta_1 r_{b2} + \beta_2 r_{b1}}, \quad (4)$$

where  $\beta_1$  and  $\beta_2$  are forward current gains,  $V_{Be1}$  and  $V_{Be2}$  are potential barriers of emitter junctions,  $r_{b1}$  and  $r_{b2}$  are base series resistances of transistors V1 and V2, respectively,  $I_s$  is current of the current source. Parameters  $r_b$ ,  $\beta$  and  $R$  are averages of  $r_{b1}$ ,  $r_{b2}$ ;  $\beta_1$ ,  $\beta_2$ , and  $R_1$ ,  $R_2$ , respectively.

The influence of the element parameters on  $U_0$  can be determined using (4). This equation can be simplified creating the equations individually for each difference of the element parameters:  $V_{Be1} - V_{Be2}$ ;  $\beta_2 - \beta_1$ ;  $r_{b1} - r_{b2}$ ;  $R_2 - R_1$ . For example, the dependence of  $U_0$  on difference  $V_{Be1} - V_{Be2}$

$$U_{0V} = V_{Be1} - V_{Be2} \quad (5)$$

was derived using (4) on condition that all parameters of arm elements are symmetric except  $V_{Be1}$  and  $V_{Be2}$ , i.e.  $\beta_1 = \beta_2 = \beta$ ,  $r_{b1} = r_{b2} = r_b$ ,  $R_1 = R_2 = R$  and  $V_{Be1} \neq V_{Be2}$ . In the same way, the  $U_0$  dependences on  $\beta_2 - \beta_1$ ,  $r_{b1} - r_{b2}$  and  $R_2 - R_1$  are:

$$U_{0\beta} = \frac{1}{2} I_s r_b (\beta_2 - \beta_1), \quad (6)$$

$$U_{0r} = \frac{1}{2} I_s \frac{1}{\beta} (r_{b1} - r_{b2}), \quad (7)$$

$$U_{0R} = \frac{1}{2} I_s r_b \frac{1}{\beta R} (R_2 - R_1). \quad (8)$$

The differentiation of equations (5)-(8) was performed with respect to the variables  $V_{Be1} - V_{Be2}$ ,  $\beta_2 - \beta_1$ ,  $r_{b1} - r_{b2}$  and  $R_2 - R_1$ , respectively, and equations of the sensitivity of  $U_0$  to variation of these variables were obtained:

$$\frac{\partial U_{0V}}{\partial (V_{Be1} - V_{Be2})} = 1, \quad (9)$$

$$\frac{\partial U_{0\beta}}{\partial (\beta_2 - \beta_1)} = \frac{1}{2} I_s r_b, \quad (10)$$

$$\frac{\partial U_{0r}}{\partial (r_{b1} - r_{b2})} = \frac{1}{2} I_s \frac{1}{\beta}, \quad (11)$$

$$\frac{\partial U_{0R}}{\partial (R_2 - R_1)} = \frac{1}{2} I_s r_b \frac{1}{\beta R}. \quad (12)$$

The input offset voltage deviation dependence on deviations of differences of the element parameters

$$\Delta U_0 = \frac{\partial U_{0V}}{\partial (V_{Be1} - V_{Be2})} \Delta V_{Be} + \frac{\partial U_{0\beta}}{\partial (\beta_2 - \beta_1)} \Delta \beta + \frac{\partial U_{0r}}{\partial (r_{b1} - r_{b2})} \Delta r_b + \frac{\partial U_{0R}}{\partial (R_2 - R_1)} \Delta R, \quad (13)$$

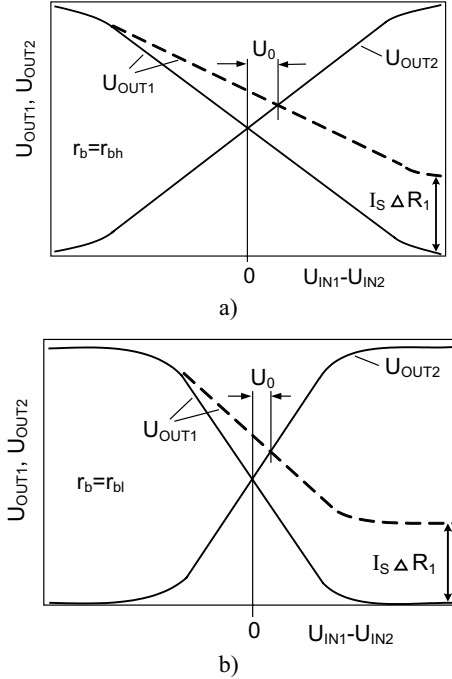
where  $\Delta V_{Be} = V_{Be1} - V_{Be2}$ ,  $\Delta \beta = \beta_2 - \beta_1$ ,  $\Delta r_b = r_{b1} - r_{b2}$ ,  $\Delta R = R_2 - R_1$  are the deviations of the element parameters.

Using equations (9)-(12) on the basis of (13)

$$\Delta U_0 = \frac{1}{2} I_s \left[ r_b \left( \Delta \beta + \frac{1}{\beta R} \Delta R \right) + \frac{1}{\beta} \Delta r_b \right] + \Delta V_{Be}. \quad (14)$$

The  $\Delta U_0$  is deviation of  $U_0$  relative to the nominal value  $U_0=0$ , i.e.  $U_0$  coincides with  $\Delta U_0$ , and because of this, equation (14) describes  $U_0$ . Obtained equation (14) shows us the ways for the input offset voltage reduction of the analogue IC based on the differential amplifiers for the case when transistors operate at high-current density. It is seen that at given current of the current source  $I_s$  and resistance of the resistors  $R_1$  and  $R_2$  the  $U_0$  can be reduced by using transistors of differential amplifier arms V1 and V2 (Fig. 1) with as low as possible base series resistance  $r_b$  and high forward current gain  $\beta$ . The explanation of the essence of this phenomenon is presented in Fig. 2. The

reduction of  $r_b$  of transistors V1 and V2 increases the steepness of the differential amplifier transfer characteristic  $U_{OUT1}, U_{OUT2} = f(U_{IN1}-U_{IN2})$ . The transfer characteristic for high and low value of  $r_b$  is presented in Fig. 2. It is seen that the influence of the same deviation of  $R_2$  resistance on  $U_0$  is different. The value of  $U_0$  decreases when  $r_b$  decreases. The increasing of the forward current gain  $\beta$  of transistors V1 and V2 has a similar influence on the decrease of  $U_0$ .

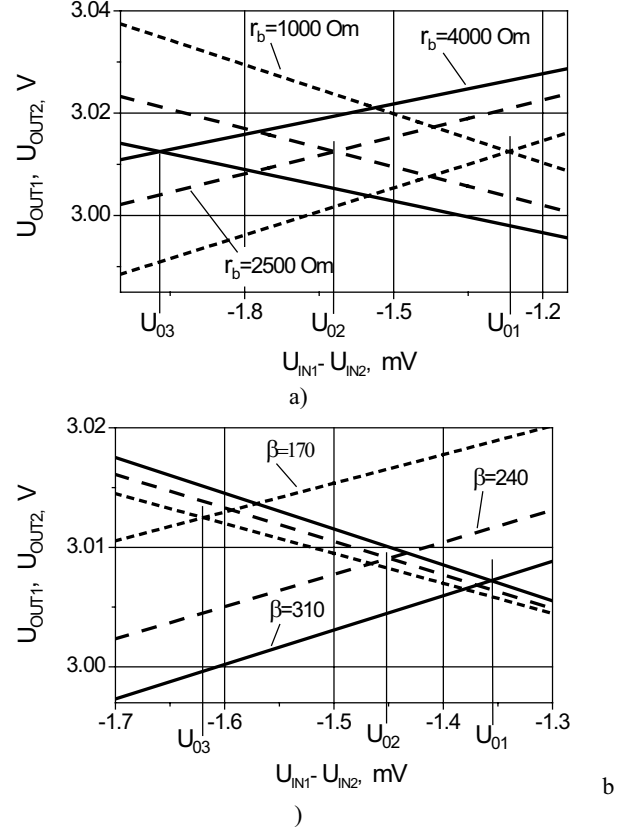


**Fig. 2.** The transfer characteristic of the differential amplifier at high value of  $r_b = r_{bh}$  (a) and low value of  $r_b = r_{bl}$  (b) at  $\Delta V_{Be}, \Delta\beta, \Delta r_b = 0$  and various  $R_1$  values:  $R_1 = R_2$  (solid line);  $R_1 = R_2 - \Delta R_1$  (dashed line)

### The numerical investigation

Obtained equations (4) and (14) used for analytical analysis are quite approximate. Therefore, it is desirable to check if the means of  $U_0$  reduction determined using these equations really work. The numerical simulation of the differential amplifier was employed for this purpose. The electronic circuit simulation software *Spice* based on the commonly accepted Gummel-Poon model of the bipolar junction transistor was used for the analysis. It has been assumed that the asymmetry of the differential amplifier is introduced by the use of resistors in the arms of the amplifier with the different resistance ( $R_1 = 2.04\text{k}\Omega$  and  $R_2 = 1.96\text{k}\Omega$ ), the supply voltage of the simulated differential amplifier  $V_{CC} = 5\text{V}$ , the input voltage  $U_{IN2} = 3\text{V}$  and current of the current source  $I_S = 2\text{mA}$ . The transfer characteristic was obtained by varying the input voltage  $U_{IN1}$ . The central fragment of the transfer characteristics of the differential amplifier, which allows us to estimate the  $U_0$ , was calculated. The influence of  $r_b$  and  $\beta$  on the  $U_0$  was investigated. The simulation was provided for the fixed  $\beta$  value ( $\beta = 170$ ) at various  $r_b$  values (Fig. 3a) and for the fixed  $r_b$  value ( $r_b = 2500\Omega$ ) at various  $\beta$  values (Fig. 3b). The values of other transistor model parameters such as the emitter junction saturation current ( $i_s$ ) and the forward

current emission coefficient ( $n_f$ ), which determine the static characteristics of the transistor operating in the forward active mode, were as follows:  $i_s = 10^{-18}\text{A}$  and  $n_f = 1$ .



**Fig. 3.** The central fragment of transfer characteristic of the differential amplifier at various values of base series resistance  $r_{b1} = r_{b2} = r_b$  (a) and forward current gain  $\beta_1 = \beta_2 = \beta$  (b) of transistors V1 and V2

The value of  $U_0$  in Fig. 3 corresponds to the value of  $U_{IN1} - U_{IN2}$ , at which  $U_{OUT1} = U_{OUT2}$ . It is seen that the decrement of  $r_b$  and increment of  $\beta$  allow us to reduce the  $U_0$  (compare  $U_0$  values  $U_{01}$ ,  $U_{02}$  and  $U_{03}$  given in Fig. 3), i.e. the obtained numerical simulation results confirm the efficiency of  $U_0$  reduction means found using proposed analytical analysis method based on derived equations (4) and (14). The values of  $U_0$  calculated on the basis of these equations are comparable to those obtained using numerical simulation. As an example, the value of  $U_0 = U_{03} = -1.9\text{mV}$ , which can be found using characteristics presented in Fig. 3a that correspond to  $r_b = 4000\Omega$ , is comparable to that  $U_0 = -1.0\text{mV}$  obtained on the basis of (4) or (14).

### Conclusions

The proposed analytical method for differential amplifier offset voltage analysis allows us to determine the input offset voltage reduction means of the differential amplifier based on the bipolar junction transistors operating at high-current density. The derived equations show that the input offset voltage can be reduced effectively by the employment of the transistors with the reduced base series resistance and high forward current gain in the differential amplifier arms.

The results gained using suggested analytical analysis method are confirmed by the numerical investigation of the differential amplifier.

## References

1. **Jasonis V., Marcinkevičius A. J.** Simulation of Transient Processes in the Fast Track-and-Hold Circuits // *Electronics and Electrical Engineering*. – Kaunas: Technologija, 2008. – No. 3(83). – P. 59–62.
2. **Wu Z. Z., Xiaoplang X. Y.** A high gain low offset amplifier with rail-to-rail inputs // *Proceedings of the Electron Devices and Solid-State Circuits conference EDSSC'05*. – Hong Kong, 2005. – P. 445–448.
3. **Matthews T. W., Heedley P. L.** A simulation method for accurately determining DC and dynamic offsets in comparators. // *Proceedings of the 48th Midwest Symposium on Circuits and Systems MWCAS'05*. – Cincinnati, Ohio, USA, 2005. – P. 1815–1818.
4. **Lee B. G., Yan S.** A new ratio-independent A/D conversion technique for high-resolution pipeline A/D converters // *Proceedings of IEEE International Symposium on Circuits and Systems ISCAS'05*. – Kobe, Japan, 2005. – P. 1960–1963.
5. **Linder M., Ingvarson F., Jeppson K.O., Grahn J. V., Zhang S. L., Ostling M.** On DC modeling of the base resistance in bipolar transistors // *Solid-St Electron*. –2000. – Vol. 44. – P. 1411–1418.
6. **Baskys A.** The model of the p–n junction depletion region v–i characteristic considering the dependence of concentration of majority carriers on voltage // *Proceedings of International Baltic Electronics conference BEC'2006*. – Tallinn, 2006. – P. 45–46.
7. **Baskys A.** Equation of the junction with extended validity area towards the high-level injection // *Electronics and Communications*. – Kiev, 2006. – No. 1. – P. 9–12.
8. **Pierret F.** Semiconductor device fundamentals. – Addison-Wesley Publishing Company, N. Y. –1996.
9. **Kašauskas V., Anilionis R., Eidukas D.** Modeling of Manufacturing Processes in EPIC Technology // *Electronics and Electrical Engineering*. – Kaunas: Technologija, 2008. – No. 7(87). – P. 49–52.
10. **Andriukaitis D.** The Adequate Selection Algorithm by Estimating Local Oxide Influence // *Electronics and Electrical Engineering*. – Kaunas: Technologija, 2010. – No. 8(104). – P. 39–42.
11. **Andriukaitis D., Anilionis R.** Investigation of Etching Process in Nano Structures // *Electronics and Electrical Engineering*. – Kaunas: Technologija, 2008. – No. 6(86). – P. 77–80.

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**A. Baskys, L. Nickelson, R. Navickas. Analytical Method for Differential Amplifier Offset Voltage Analysis // Electronics and Electrical Engineering. – Kaunas: Technologija, 2011. – No. 2(108). – P. 51–54.**

The analytical method for differential amplifier offset voltage analysis is presented in the work. The method is developed for the amplifier based on the bipolar junction transistors that operate at high-current density. The transistor model based on the equation of the junction, which takes into account the dependence of majority carrier boundary concentrations on junction voltage that should be considered at high-current density, is used as the base for derivation of input offset voltage equations. The derived equations are valid in the narrow region of current, at which the differential amplifier input offset voltage measurement is provided. The obtained equations allow us to estimate the input offset voltage reduction ways. The results gained using suggested analytical analysis method are confirmed by the numerical investigation of the differential amplifier. Ill. 3, bibl. 11 (in English; abstracts in English and Lithuanian).

**A. Baskys, L. Nickelson, R. Navickas. Analitinis diferencinio stiprintuvo nulinio poslinkio įtampos analizės metodas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2011. – Nr. 2(108). – P. 51–54.**

Darbe pateiktas analitinis diferencinio stiprintuvo su dvipoliais tranzistoriais, kurie veikia esant dideliame srovės tankiui, nulinio poslinkio įtampos analizės metodas. Nulinio poslinkio įtampos išraiškoms gauti panaudotas dvipolio tranzistoriaus modelis, sukurtas naudojant pn sandūros modelį, kuriame įvertintas svarbiausias sandūros efektas, pasireiškiantis esant dideliems srovės tankiams, – pagrindinių krūvininkų tankio priklausomybė nuo sandūros įtampos. Išvestos išraiškos galioja siaurame srovės diapazone, kuriame veikia tranzistoriai matuojant nulinio poslinkio įtampą. Gautos išraiškos leidžia nustatyti diferencinio stiprintuvo nulinio poslinkio įtampos mažinimo būdus. Skaitmeninis tyrimas patvirtina rezultatus, gautus naudojant pasiūlytą diferencinio stiprintuvo analitinės analizės metodą. Il. 3, bibl. 11 (anglų kalba; santraukos anglų ir lietuvių k.).