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Procedia Computer Science 184 (2021) 17–23

Procedia Computer Science

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The 12th International Conference on Ambient Systems, Networks and Technologies (ANT)
March 23-26, 2021, Warsaw, Poland

Comparison of parameters of ring and LC-tank digitally controlled oscillators in 0.13 μm CMOS

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Abstract

Integrated circuits (IC) of two digitally controlled oscillators (DCO) are presented in this article – ring and LC-tank oscillator. Main parameters of these DCOs are measured and compared, applications of such DCOs are discussed. Ring DCO is made of 48 sections of 3-stage ring oscillators. Base component of ring oscillator is tristate inverter, which is accessible in modern CMOS technologies, therefore, such oscillator can be implemented using digital IC design tools. Main components of LC-tank DCO are inductor, switched-capacitor bank, and a pair of cross-coupled NMOS transistors. Frequency of ring DCO is controlled by enabling or disabling its separate sections, while frequency of LC DCO is controlled by switching capacitors of LC tank. Although LC DCO is controlled digitally, its core is analog and it can be implemented only using custom design tools. Both DCOs are designed and their prototypes are manufactured in mature and low-cost 0.13 μm RF CMOS technology. Ring DCO's frequency tuning range is 370–873 MHz; phase noise at maximum operating frequency at 1 MHz offset from carrier is –109.19 dBc/Hz; power consumption is 3.6 mW; used area of silicon is 0.0065 mm^2. LC-tank DCO's frequency tuning range is 9.26–10.58 GHz; phase noise at maximum operating frequency at 1 MHz offset from carrier is –106.46 dBc/Hz; power consumption is 18 mW; used area of silicon is 0.06 mm^2. Operating frequency of LC-tank DCO is much higher, however Figures of Merit of ring and LC-tank DCOs are comparable and respectively equal to –140.61 dBc/Hz and –136.88 dBc/Hz. It shows, that both DCOs can be used in modern systems for appropriate applications. Main applications of LC-tank DCO are high-speed systems, where high frequency is needed, while in low-cost, low-power systems ring DCO is more suitable.

Keywords: Digitally controlled oscillator; LC-tank oscillator; Integrated circuit; Ring oscillator

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10.1016/j.procs.2021.04.019

1. Introduction

Development, research and implementation of wireless technologies is growing vigorously in recent years – mobile 5G systems are being deployed, many conventional devices and appliances are getting connectivity and becoming part of Internet of Things (IoT) systems, which improve and make everyday tasks easier, various wireless technologies are used in Intelligent Transport Systems (ITS) to improve road safety and make our travels faster, etc. [1–3].

In complex systems, such as ITS, various devices can be used – from high-speed communication transceivers to low-power sensors. However, at the core of any wireless or smart device there is frequency synthesiser, which generates high frequency signal for a carrier or clock signal for synchronization of all circuits. Each Frequency synthesiser has at least one oscillator. Usually LC-tank voltage-controlled oscillators are used for wireless applications, but with development of Integrated Circuit technologies all-digital frequency synthesisers are gaining popularity which uses digitally controlled oscillator (DCO) [4].

There are two main types of digitally controlled oscillators – LC-tank DCO, which is digital counterpart of LC-tank voltage-controlled oscillator, and ring DCO. In this paper we present structures of designed both, LC-tank and ring, DCOs in exactly the same 0.13 μm RF CMOS technology, their parameters and carry out quantitative comparison of these DCOs. Also, main applications of both DCOs are discussed.

2. Design of ring and LC-tank digitally controlled oscillators

2.1. Structure of ring oscillator

Structure of the designed ring oscillator is shown in Fig. 1. The base is three-stage oscillator. Stages are made of tri-state inverters, which are available as a standard cells in process design kits of modern integrated circuit (IC) manufacturing technologies, what makes possible to implement such oscillator in hardware description language, what in-turn allows automatic synthesis and place and route of such IC [5,6]. In this case it was implemented in VHDL. Also, such implementation enables easy migration to other technology nodes.

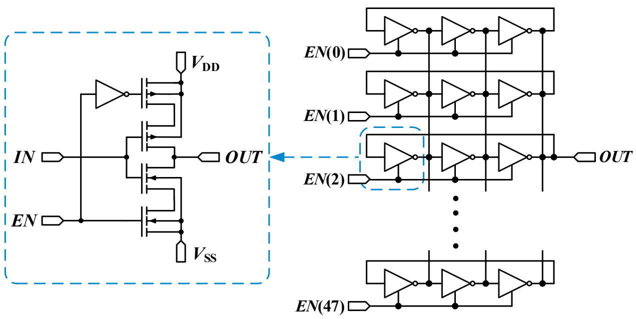


Fig. 1. Structure of designed ring oscillator.

The designed digitally controlled ring oscillator is made of 48 sections of three-stage oscillator. All respective stages of each section are connected in parallel. Each stage can be disabled or enabled individually. If logic value of control bit of the stage is low, outputs of the inverters are set to high impedance state - this stage is disabled. If logic value of control bit of the stage is high, inverters are enabled. Because all respective inverters in different sections are connected in parallel, by enabling section effective driving power of each stage is increased thus increasing its speed and frequency of oscillation. Highest operating frequency is set when all 48 stages of ring oscillator are enabled. If all sections are disabled, the ring oscillator stops oscillating and enters turned-off state.

2.2. Structure of LC-tank oscillator

Structure of designed LC-tank digitally controlled oscillator is shown in Fig. 2. This structure of DCO is described in details in [7]. Main parts of this oscillator are high quality inductor, switched-capacitor bank, and pair of cross–coupled NMOS transistors that provide negative resistance to the tank. Inductor together with bank of capacitors assemble LC tank of the oscillator. Since inductor takes large area of silicon, frequency of the LC DCO is controlled by changing capacitance of the LC tank – if larger number of capacitors is connected, frequency of oscillations decreases. Switched capacitors are controlled using 6-bit binary code.

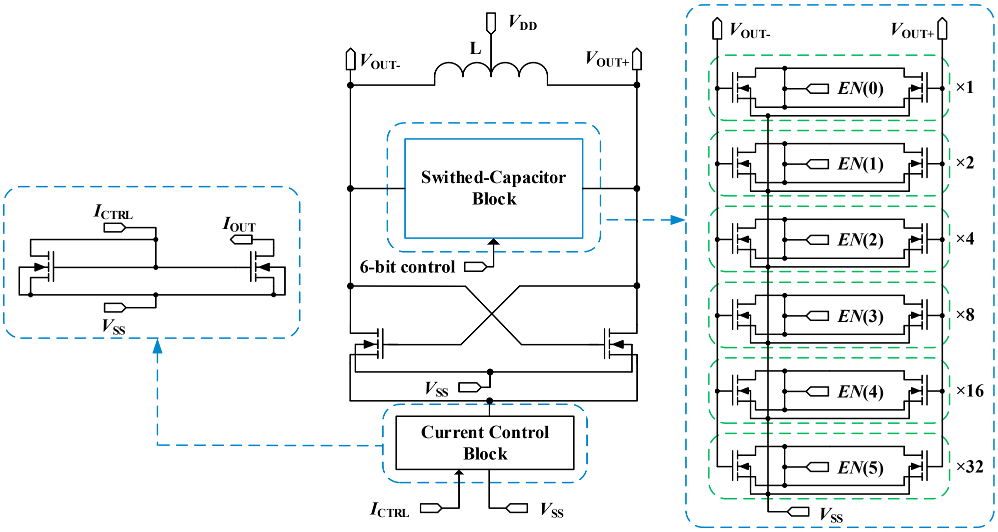


Fig. 2. Structure of designed LC-tank Digitally Controlled Oscillator.

Current Control Block, which is based on current mirror, is used to regulate the bias point of LC DCO and optimize swing of an output signal of the DCO.

Although such oscillator is controlled digitally, its core is based on analog design. Therefore, automatic synthesis cannot be applied for it and design process of such DCO is mainly manual and labour-intensive.

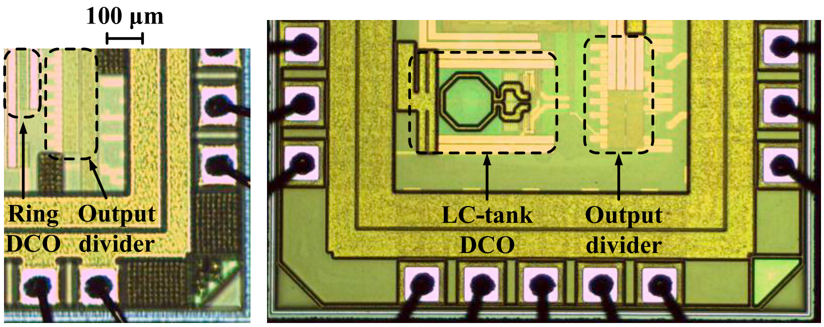
2.3. Output divider

To relieve requirements for packaging and design of evaluation board of the prototype, frequency divider is used at the output of both DCOs.

Structure of divider for both DCOs is the same. It consists of eight divide-by-2 stages, which are connected in series. Such structure results in frequency division ratio of 256. Divide-by-2 cells are based on ETSPC (Extended True Single-Phase Clock), flip-flops. Such flip-flops and dividers became popular in recent years, because of their low complexity, high operating frequency, low power consumption and small used area of silicon, compared to other commonly used dividers, such as CML (Current Mode Logic), Razavi, Wang topologies [8,9].

3. Measurement results

Prototypes of digitally controlled ring oscillator and LC-tank oscillator were designed and manufactured in mature low-cost 0.13 µm RF CMOS technology. Micrographs of manufactured prototypes of ring and LC-tank oscillators are presented respectfully in Fig. 3 (a) and (b). Used area of silicon of ring DCO and LC DCO is respectively 130 µm × 50 µm and 193 µm × 311 µm.

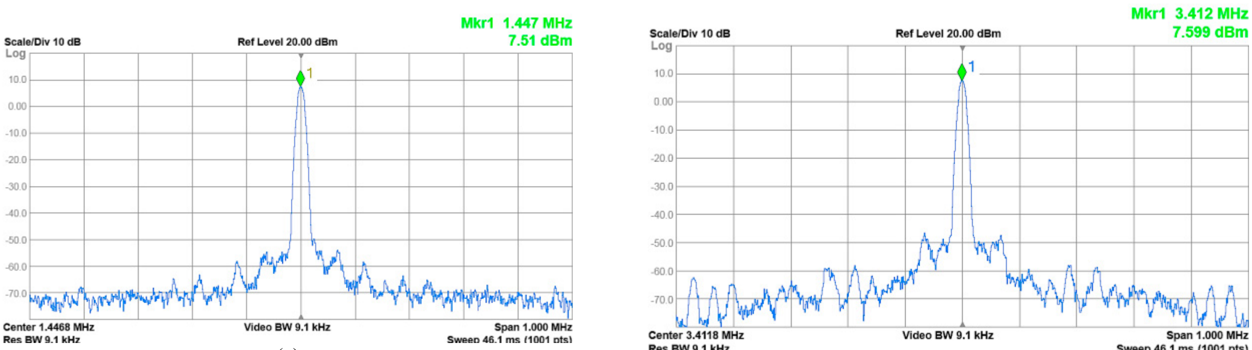


(a) (b)

Fig. 3. Micrographs of ring DCO (a) and LC-tank DCO (b)

With a supply voltage of ring DCO of 1.2 V, current consumption at the highest operating frequency is 3 mA.

Frequency tuning range of ring DCO is from 370 MHz to 873 MHz, what results in relative tuning range equal to 80.9 %. Frequency spectrum at the divide-by-256 output of ring DCO, when it operates at lowest and highest operating frequency, is shown in Fig. 4. Oscillations starts when at least 4 sections of oscillator are enabled. Measurement results of phase noise of ring DCO at highest operating frequency is shown in Fig. 5. Phase noise at the divider's output at highest operating frequency at 1 MHz offset from the carrier is equal to –133.19 dBc/Hz. It should be noted that each divide-by-2 cell improves phase noise by 3 dBc/Hz [10]. Used frequency divider is made of eight divide-by-2 cells, therefore phase noise at the output of ring DCO is equal to –109.19 dBc/Hz.



(a) (b)

Fig. 4. Measured frequency spectrum at the divide-by-256 output of ring DCO at (a) lowest operating frequency; (b) highest operating frequency

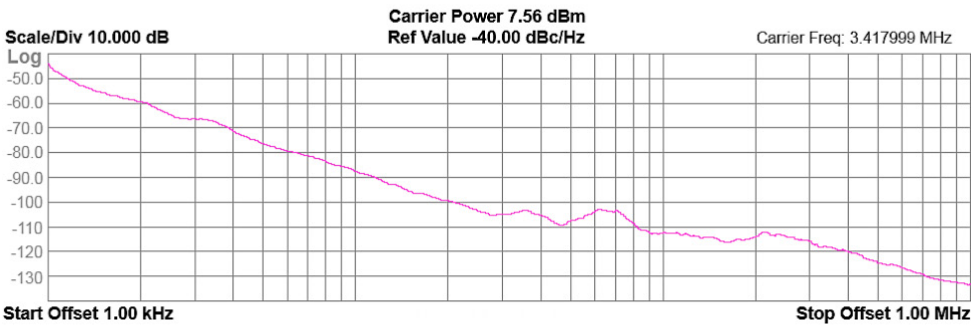


Fig. 5. Measurement results of phase noise at highest operating frequency at the divide-by-256 output of the designed ring DCO

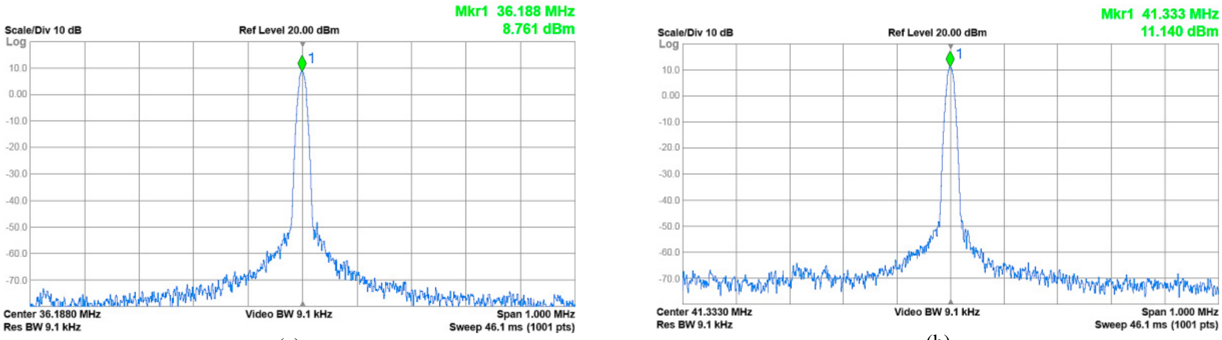


Fig. 6. Measured frequency spectrum at the divide-by-256 output of LC-tank DCO at (a) lowest operating frequency; (b) highest operating frequency

With a supply voltage of LC DCO of 1.8 V, current consumption at the highest operating frequency is 10 mA.

Frequency tuning range of LC DCO is from 9.26 GHz to 10.58 GHz, what results in relative tuning range equal to 13.3 %. Frequency spectrum at the divide-by-256 output of LC DCO, when it operates at lowest and highest operating frequency, is shown in Fig. 6. Measurement results of phase noise of LC DCO at highest operating frequency is shown in Fig. 7. Phase noise at the divider's output at highest operating frequency at 1 MHz offset from the carrier is equal to –130.46 dBc/Hz and phase noise at the output of LC DCO is equal to –106.46 dBc/Hz.

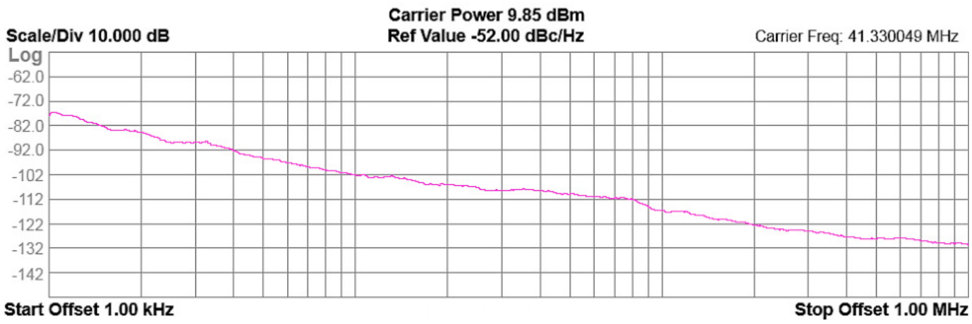


Fig. 7. Measurement results of phase noise at highest operating frequency at the divide-by-256 output of the designed LC DCO

Summary of parameters of both DCOs and comparison to other works is presented in Table 1. Figure of Merit (FOM) is used for quantitative comparison of DCOs. Commonly used FOM, which is shown in equation (1), combine all main parameters of DCO [11].

$$FOM_{\mathrm{T}} = PN(\Delta f) - 20\log\left(\frac{F_0 \cdot \Delta F}{\Delta f \cdot 10}\right) + 10\log\left(\frac{P}{1\ \mathrm{mW}}\right), \tag{1}$$

where F_0 is a carrier frequency, $PN(\Delta f)$ is a phase noise at an offset frequency Δf from the carrier frequency, ΔF is a relative tuning range, P is a power consumption in mW.

As it is seen from the provided parameters of ring DCO and LC DCO, operating frequency of the LC DCO in same technology is much higher, compared to operating frequency of ring DCO. However, ring DCO has wider relative tuning range, lower power consumption and smaller used area of silicon. Phase noise at highest operating frequency of both DCOs at 1 MHz offset from the carrier is comparable. Therefore, despite large difference in operating frequency, FOM of both DCOs is comparable.

Table 1. Summary of parameters of designed ring and LC-tank DCOs and comparison to other works.

Parameter	This Work		[12]	[13]	[14]	[15]	[16]	[17]
Type of the DCO	Ring	LC-tank	LC-tank	LC-tank	LC-tank	Ring	Ring	Ring
CMOS technology node	0.13 μm		65 nm	0.13 μm	55 nm	28 nm	65 nm	65 nm
Minimum operating frequency F_{min}, GHz	0.37	9.26	13.69	1.99	9.60	1.13	1.80	0.90
Maximum operating frequency F_{max}, GHz	0.87	10.58	15.93	2.50	10.50	1.54	2.20	1.40
Center frequency F_c, GHz	0.62	9.92	14.81	2.25	10.05	1.34	2.00	1.15
Relative tuning range ΔF	0.81	0.13	0.15	0.23	0.09	0.31	0.20	0.43
Phase noise measurement frequency F_0, GHz	0.87	10.58	15.00	2.19	10.00	1.31	2.20	1.25
Phase noise at 1 MHz offset PN(1 MHz), dBc/Hz	-109.2	-106.5	-99.0	-107.0	-106.3	-74.0	-78.9	-96.50
Supply voltage V_{DD}, V	1.2	1.8	1.2	1.2	1.2	1.0	1.2	0.9
Power dissipation P, mW	3.6	18.0	19.8	15.2	7.3	0.8	1.6	2.3
Used area S, μm^2	130 × 50	193 × 311	N/A	$4.3\cdot10^5$	N/A	52 × 108	26 × 14	90 × 210
Figure of Merit FOM_T, dBc/Hz	-140.61	-136.88	-133.67	-130.26	-137.13	-108.25	-109.73	-128.67

These parameters show, that both DCOs can be used in modern systems – LC-tank DCO can be used for high-speed systems, where frequency is prioritised e.g., modern wireless transceivers; ring DCO can be used in low-cost, low-power devices, such as sensors. However, it is seen and should be noted, that with rapid development of CMOS manufacturing technologies, operating frequency of logic gates and ring DCO, which is based on them, is improving on smaller technology nodes [18].

4. Conclusions

In this paper ring and LC-tank digitally controlled oscillators are presented. Both oscillators are designed, and their prototypes are manufactured in the same 0.13 μm RF CMOS technology.

Structure of ring DCO is composed of 48 sections of three-stage digitally controlled oscillators, whose corresponding stages are connected in parallel. Frequency of this DCO is controlled by enabling or disabling its sections. Main component of oscillator's stage is tristate inverter, which is available as standard cell in modern CMOS technologies. Such DCO, due to its structure, can be designed and synthesised using digital IC design tools.

Main components of LC-tank DCO are inductor, switched-capacitor bank and pair of cross-coupled transistors. Frequency of this DCO is controlled by switching capacitors of LC-tank. Although such DCO is controlled by digital code, its core is analog. Therefore, design process of such DCO is manual and labour-intensive.

Frequency tuning range of ring and LC-tank DCO is respectfully 370–873 MHz and 9.26–10.58 GHz. Power dissipation at highest operating frequency of ring and LC-tank DCO is respectfully 3.6 mW and 18 mW. Used are of silicon of ring and LC-tank DCO is respectfully 130 μm × 50 μm and 193 μm × 311 μm. Phase noise at highest operating frequency at 1 MHz offset from the carrier of ring and LC-tank DCO is respectfully –109.19 dBc/Hz and –106.46 dBc/Hz.

Operating frequency of LC-tank DCO, compared to ring DCO, is more than 11 times higher. However, its relative tuning range is lower, power dissipation and used area of silicon is higher. Phase noise of both oscillators is comparable. Calculated Figure of Merit is also similar for both DCOs, what shows, that both oscillators can be used in modern systems: LC tank DCO is preferrable for high-speed applications, where requirements for operating frequency are higher, while ring DCO can be used for low-cost, low-power applications, due to its smaller space, lower current consumption and relatively easier design process.

Acknowledgements

The team of authors wishes to express their gratitude for financial support of this research. This project has received funding from European Regional Development Fund (project No 01.2.2-LMT-K-718-01-0054) under grant agreement with the Research Council of Lithuania (LMTLT).

References

[1] Manyika J, Chui M, Bisson P, Woetzel J, Dobbs R, Bughin J, et al. The Internet of Things: Mapping the value beyond the hype. New York: 2015.

[2] Siow E, Tiropanis T, Hall W. Analytics for the Internet of Things. ACM Comput Surv 2018;51:1–36. https://doi.org/10.1145/3204947.

[3] Kiela K, Barzdenas V, Jurgo M, Macaitis V, Rafanavicius J, Vasjanov A, et al. Review of V2X–IoT Standards and Frameworks for ITS Applications. Appl Sci 2020;10:4314. https://doi.org/10.3390/app10124314.

[4] Babaie M, Ferreira SB, Kuo F, Staszewski RB. A 4.4mW-TX, 3.6 mW-RX Fully Integrated Bluetooth Low Energy Transceiver for IoT Applications. Hybrid ADCs, Smart Sensors IoT, Sub-1V Adv. Node Analog Circuit Des., Cham: Springer International Publishing; 2018, p. 335–59. https://doi.org/10.1007/978-3-319-61285-0_18.

[5] Park Y, Wentzloff DD. A cyclic vernier TDC for ADPLLs synthesized from a standard cell library. IEEE Trans Circuits Syst I Regul Pap 2011;58:1511–7. https://doi.org/10.1109/TCSI.2011.2158490.

[6] Jurgo M, Navickas R. Synthesizable 2D Vernier TDC based on gated ring oscillators. Inf MIDEM 2017;47:223–31.

[7] Macaitis V, Navickas R. Design of High Frequency, Low Phase Noise LC Digitally Controlled Oscillator for 5G Intelligent Transport Systems. Electronics 2019;8:72. https://doi.org/10.3390/electronics8010072.

[8] Jurgo M, Kiela K, Navickas R. Design of Low Noise 10 GHz divide by 16…511 Frequency Divider. Electron Electr Eng 2013;19:87–90. https://doi.org/10.5755/j01.eee.19.6.4570.

[9] Heydarzadeh S, Torkzadeh P, Pourmina M. A 12GHz programmable fractional-n frequency divider with 0.18um CMOS technology. 2013 5th Comput. Sci. Electron. Eng. Conf., IEEE; 2013, p. 29–33. https://doi.org/10.1109/CEEC.2013.6659440.

[10] Apostolidou M, Baltus PGM, Vaucher CS. Phase noise in frequency divider circuits. 2008 IEEE Int. Symp. Circuits Syst., IEEE; 2008, p. 2538–41. https://doi.org/10.1109/ISCAS.2008.4541973.

[11] Cheng KH, Tsai YC, Lo YL, Huang JS. A 0.5-V 0.4-2.24-GHz inductorless phase-locked loop in a system-on-chip. IEEE Trans Circuits Syst I Regul Pap 2011;58:849–59. https://doi.org/10.1109/TCSI.2010.2089559.

[12] Lou L, Bo Chen, Kai Tang, Yuanjin Zheng. A CMOS digital-controlled oscillator for All-digital PLL frequency synthesizer. 2016 Int. Symp. Integr. Circuits, IEEE; 2016, p. 1–4. https://doi.org/10.1109/ISICIR.2016.7829720.

[13] Samarah A, Carusone AC. A digital phase-locked loop with calibrated coarse and stochastic fine TDC. IEEE J Solid-State Circuits 2013;48:1829–41. https://doi.org/10.1109/JSSC.2013.2259031.

[14] Pu Z, Gai W, Shi L, He A, Feng J. A 10GHz Class-C Digitally-Controlled Oscillator with Fast Start-up Dynamic Biasing. 2019 IEEE Int. Conf. Electron Devices Solid-State Circuits, IEEE; 2019, p. 1–2. https://doi.org/10.1109/EDSSC.2019.8754454.

[15] Bisiaux P, Blokhina E, Koskin E, Siriburanon T, Galayko D. Design of a 1.5 GHz Low jitter DCO Ring in 28 nm CMOS Process. ECCTD 2020 - 24th IEEE Eur Conf Circuit Theory Des 2020:4–8. https://doi.org/10.1109/ECCTD49232.2020.9218352.

[16] Selvaraj S, Bayram E, Negra R. Low phase noise, high resolution digitally-controlled ring oscillator operating at 2.2GHz. 2020 9th Int. Conf. Mod. Circuits Syst. Technol., IEEE; 2020, p. 1–4. https://doi.org/10.1109/MOCAST49295.2020.9200272.

[17] Yuan C, Shekhar S. A Supply-Noise-Insensitive Digitally-Controlled Oscillator. IEEE Trans Circuits Syst I Regul Pap 2019;66:3414–22. https://doi.org/10.1109/TCSI.2019.2924399.

[18] Jurgo M, Navickas R. Comparison of TDC parameters in 65 nm and 0.13 μm CMOS. 2017 5th IEEE Work. Adv. Information, Electron. Electr. Eng., IEEE; 2017, p. 1–4. https://doi.org/10.1109/AIEEE.2017.8270544.